

S/N 09/602374



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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Ruutu, et al
Serial No.: 09/602374 Group Art Unit: 2731
Filed: 6/23/00 Docket No.: 975.305USW1
Title: CLOCK GENERATING METHOD AND APPARATUS FOR AN
ASYNCHRONOUS TRANSMISSION

CERTIFICATE UNDER 37 C.F.R. 1.8: The undersigned hereby certifies that this Transmittal Letter and the paper, as described herein, are being deposited in the United States Postal Service, as first class mail, with sufficient postage, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on November 13, 2000.

Iain A. McIntyre
Name

Signature

Group Art Unit 2731
Assistant Commissioner for Patents
Washington, D.C. 20231

- ☒ Certified copy of WIPO Serial Number PCT/EP 97/07264, filed 23 December 1997; Submission of Priority Document
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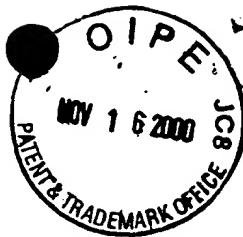
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Date: November 13, 2000

By:

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S/N 09/602374



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Group Art Unit 2731
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Enclosed is a certified copy of WIPO application, Serial Number PCT/EP 97/07264, filed 23 December 1997, the priority of which is claimed under 35 U.S.C. §119.

Respectfully submitted,

Altera Law Group, LLC
10749 Bren Road East, Opus 2
Minneapolis, MN 55343
(952)-912-0571

Date: Nov 13, 2000

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Im Auftrag
For the President of the European Patent Office
Le Président de l'Office européen des brevets
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Patentanmeldung Nr.
Patent application no.
Demande de brevet n°

PCT/EP 97/07264

Blatt 2 der Bescheinigung
Sheet 2 of the certificate
Page 2 de l'attestation



Anmeldung Nr.: PCT/EP 97/07264
Application no.:
Demande n°:

Anmelder: 1. NOKIA TELECOMMUNICATIONS OY - Nokia Group, Finland
Applicant(s): 2. RUUTU, Jussi - Helsinki, Finland
Demandeur(s): 3. KAARESOJA, Topi - Helsinki, Finland

Bezeichnung der Erfindung:
Title of the invention: Clock generating method and apparatus for an asynchronous transmission
Titre de l'invention:

Anmeldetag:
Date of filing: 23 December 1997 (23.12.97)
Date de dépôt:

In Anspruch genommene Priorität(en)
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Staat:	Tag:	Aktenzeichen:
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Pays:	Date:	Numéro de dépôt:

Benennung von Vertragsstaaten : Siehe Formblatt PCT/RO/101 (beigefügt)
Designation of contracting states : See Form PCT/RO/101 (enclosed)
Désignation d'états contractants : Voir Formulaire PCT/RO/101 (ci-joint)

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FIELD OF THE INVENTION

The present invention relates to a method and apparatus for generating a clock for an asynchronous transmission, to be
5 used especially in an ATM (Asynchronous Transfer Mode) connection between two devices of a Base Station Subsystem (BSS) in a GSM network.

BACKGROUND OF THE INVENTION

10

Usually, two elements of a Base Station Subsystem (BSS) in a GSM network are connected via a synchronous PCM connection. The principle of such an STM connection (Synchronous Transfer Mode) is shown in Fig. 1A. One of the devices, i.e. a
15 transmitter 1, is selected as a master and its clock is used to synchronize PCM frames sent over the connection. The second device, i.e. a receiver 2, has a slave function, since its own clock is synchronized to the master clock of the transmitter.

20

In future ATM based GSM networks, a transcoder (TC) and a Base Transceiver Station (BTS) are connected via an asynchronous ATM connection, wherein synchronization is not available at the receiver 2. In an ATM connection, bit
25 streams of binary signals of different channels are divided into unitary ATM cells to be transmitted in a time divisional manner. The cell rate defines the total number of ATM cells per second.

30 Fig. 1B shows the principle of such an ATM connection, wherein a transmitting clock generator 3 and a receiving

clock generator 4 are not synchronized and operate independently.

However, without a synchronization, the frequencies of the
5 transmitting clock and the receiving clock are not equal.
Therefore, a buffer of the receiver 2 may be filled gradually
and a buffer overflow may occur, if the transmitting clock of
the transmitter 1 is faster than the receiving clock of the
receiver, since the buffer reading speed is slower than the
10 writing speed. On the other hand, if the transmitting clock
is slower than the receiving clock, the receiver 2 may run
out of data (buffer underflow).

Both cases can result in lost data and, in case of time
15 sensitive applications like GSM speech, cumulative delay that
can rapidly become irritating. Thus, buffer underflow as well
as buffer overflow is audible.

It is therefore an object of the present invention to provide
20 a clock generating method and apparatus for an asynchronous
transmission, by means of which clock synchronization between
a transmitter and a receiver can be maintained.

This object is achieved by a clock generating method for an
25 asynchronous transmission, comprising the steps of:

determining a plurality of actual signal arrival times;
averaging said plurality of actual signal arrival
times; and

correcting a timing of a receiving clock on the basis
30 of said average of the signal arrival times and an expected
signal arrival time.

Furthermore, the above object is achieved by a clock generating apparatus for an asynchronous transmission, comprising:

5 determining means for determining an average of actual signal arrival times and for generating a control signal on the basis of said average of the actual signal arrival times and an expected signal arrival time; and

correcting means for correcting a timing of a receiving clock on the basis of said control signal.

10

Accordingly, since the timing of the receiving clock is corrected on the basis of an average of the actual arrival times of the signal and an expected arrival time, the receiving clock can be adjusted such that the expected arrival time coincides with the actual arrival time.

15

Moreover, by averaging the actual arrival time, delay variations upon signal transmission, which might cause synchronization errors, can be eliminated or at least significantly reduced.

20

Preferred developments of the present invention are defined in the subclaims.

25

BRIEF DESCRIPTION OF THE DRAWINGS

In the following, the invention and a preferred embodiment thereof will be described in greater detail with reference to the accompanying drawings in which:

30

Fig. 1A shows an STM transmission principle according to the prior art,

Fig. 1B shows an ATM transmission principle according to the prior art,

5 Fig. 2 shows a time chart for explaining an actual and an expected arrival time,

Fig. 3 shows a block diagram of a clock generating apparatus according to the preferred embodiment of the present
10 invention,

Fig. 4 shows a flow diagram of a clock generating method according to the preferred embodiment of the present invention, and

15

Fig. 5 shows a block diagram of a determining means of the clock generating apparatus according to the preferred embodiment of the present invention.

20

DESCRIPTION OF THE PREFERRED EMBODIMENT

The following preferred embodiment relates to an ATM connection between two devices of a Base Station Subsystem (BSS) in a GSM network as described above.

25

In the GSM network, a full rate TRAU (Transcoder and Rate Adaption Unit) frame is packed inside one ATM cell. The TRAU frame is an information packet transferred between the TC and the BTS and may contain 20 ms of coded speech. Thus, the ATM
30 cells are transmitted with an intervall of 20 ms corresponding to a cell rate $r = 50$ cells/s. The clock frequencies f_t , f_r of the transmitter 1 and the receiver 2

can be obtained from the cell rate r using $f_{t,r} = R \cdot r$, wherein R denotes the ratio between the clock frequency and the cell rate. For simplicity, it is assumed in the following that the clock frequencies f_t , f_r of the transmitter 1 and the
5 receiver 2 are equal to the cell rate ($R=1$).

Fig. 2 shows an example for actual arrival times t_{i-1} and t_i of two adjacent cells $i-1$ and i at the receiver 2. According to the clock of the receiver 2, the cell i is expected to
10 arrive after an interval Δt_r . However, due to a difference in the clock frequencies of the transmitter 1 and receiver 2, the cell i actually arrives after an interval Δt_t shorter than the expected interval Δt_r . Thus, in the present case, the clock frequency f_t of the transmitter 1 is higher than
15 the clock frequency f_r of the receiver 2.

Accordingly, from the viewpoint of the receiver 2, the transmitter 1 is transmitting at a cell rate higher than 50
cells/s.

20 On the other hand, the clock frequency f_t of the transmitter 1 may be lower than the clock frequency f_r of the receiver 2. In this case, the interval Δt_t is longer than the expected interval Δt_r and, from the viewpoint of the receiver 2, the
25 transmitter 1 is transmitting at a cell rate lower than 50 cells/s.

In order to recover synchronization, the clock frequency f_r of the receiver 2 has to be corrected so as to be equal to
30 the clock frequency f_t of the transmitter 1. Thus:

$$f_r^{corr} = f_r = \frac{1}{\Delta t_r} \quad (1)$$

The correction can be performed on the basis of the difference Δf between the clock frequencies f_t and f_r , which
5 can be obtained as follows:

$$\Delta f = f_t - f_r = \frac{1}{\Delta t_t} - \frac{1}{\Delta t_r} = \frac{\Delta t_r - \Delta t_t}{\Delta t_t \Delta t_r} = \frac{C - \Delta t_t}{\Delta t_t C} \quad (2)$$

wherein the constant C represents the time interval Δt_r , which
10 is fixed from the viewpoint of the receiver 2, assuming that the frequency f_r of the receiving clock does not vary. It is to be noted that Δf may also be a negative, if $f_t < f_r$.

As already mentioned, according to the GSM specifications,
15 the cell rate is 20 ms during normal speech transmission. Thus, the constant C is set to 20 ms. In case of Discontinuous Transmission (DTX), only TRAU frames containing a comfort noise information are sent every 480 ms, which means that, in this case, C has to be set to 480 ms.

20

In order to perform correction, the above frequency difference Δf has to be added to the frequency f_r of the receiving clock of the receiver 2, so that the receiver 2 operates substantially at the same frequency as the
25 transmitter 1. Thus, the corrected clock frequency f_r^{corr} of the receiver 2 can be obtained as follows:

$$f_r^{corr} = f_r + \frac{C - \Delta t_t}{\Delta t_t C} \quad (3)$$

Here, it is assumed that the difference between the time intervals Δt_r and Δt_t only results from a clock difference between the transmitter 1 and the receiver 2.

5

However, the above time difference between the actual and expected arrival times is not only caused by the difference between the clock frequencies f_r and f_t but also by a signal delay due to the signal propagation via the ATM network.

10 Namely, an ATM cell carrying a TRAU frame has a so-called time-dependent Cell Delay Variation (CDV) caused by the ATM network.

Thus, the time interval Δt_t actually results from the sum of
15 the instantaneous CDV and the clock period of the transmitter, and can be obtained as follows:

$$\Delta t_i = \Delta t_{CDV}^i + \frac{1}{f_i} \quad (4)$$

20 wherein the index i denotes an i th cell.

However, if the actual arrival time is largely affected by the CDV, the receiving clock is mainly adjusted to the more or less random CDV and not to the transmitting clock.

25 Nevertheless, in view of the fact that the CDV is randomly distributed with a mean value of zero, the CDV can be eliminated by obtaining an average Δt_i^{ave} over a certain number N of samples.

By replacing Δt_i by Δt_i^{ave} in equation (3), a good estimation of the actually required corrected frequency of the receiving clock can be obtained as follows:

$$5 \quad f_r^{corr} = f_r + \frac{C - \Delta t_i^{ave}}{\Delta t_i^{ave} C} \quad (5)$$

The average value Δt_i^{ave} is calculated as follows:

$$10 \quad \Delta t_i^{ave} = \frac{1}{N} \sum_{i=1}^N \Delta t_{CDV}^i + \frac{1}{N} \sum_{i=1}^N \frac{1}{f_i}, \quad (6)$$

wherein N should be selected such that the first sum of equation (6) can be neglected.

15 The practical value of N depends on the magnitude of the CDV and the desired accuracy and may be in a range between 100 and 10^5 . In the present speech channel, $N=100$ corresponds to 2 seconds of speech. Thus, a practical value could be $N=10^4$ corresponding to 3 min of speech, which can be achieved
20 during a telephone call. If the present invention is applied to transmission with higher bit rates, N can be chosen even larger.

During the Discontinuous Transmission (DTX), where $C=480$ ms,
25 N could be incremented by one every 20ms or by 24 every 480ms during the calculation of the above sums.

However, if N is too small, the resulting difference between the actual and the expected arrival time of the cells may even increase due to the random distribution of the CDV.

5 Fig. 3 shows a block diagram of the preferred embodiment. The receiving clock of the receiver 2 is corrected by means of a voltage controlled oscillator (VCO) 40 or any other controllable signal generator. A control signal supplied to the VCO 40 is derived from the output of a determining means
10 20 to which the actual receiving clock and the receiving signal, i.e. ATM cells, are supplied and which generates an output signal according to the above equation (5).

The output signal of the determining means 20 can be supplied
15 to the VCO 40 via an integrator 30 so as to improve accuracy and stability of correction.

Fig. 4 illustrates a flow chart of the signal processing steps performed in the determining means 20.

20 At first, in step 100, a counting variable i is set to 0 and a timer implemented by hardware or software is started when the first ATM cell is received. Subsequently, the timer is stopped when the next ATM cell is received to thereby obtain
25 the value of Δt_i as a result of counting (step 101). The obtained value of Δt_i is stored (step 102) and the timer is reset and started again when a new cell is received, wherein the value i is incremented (step 103).

30 In step 104, it is determined whether i has reached the value N, i.e. whether N samples have been stored. If so, the average value Δt_i^{ave} is calculated in step 105 by adding the

stored values of Δt_i and deviding the sum by N. In case i is smaller than N, the flow returns to step 101 in order to repeat steps 101 to 104 until i equals N.

5 After the average value Δt_i^{ave} has been calculated, the correction value for the frequency f_r of the receiving clock is calculated in accordance with equation (5). The obtained correction value is used to control the VCO 40 or any other clock generation means.

10

The determining means 20 may be constituted as shown in Fig. 5. A detecting means 21 is provided for detecting the actual arrival time of ATM cells. In accordance with the above described steps, the detecting means may comprise a timer.

15 The obtained values of Δt_i are stored in a storing means 22 in order to be used by an averaging means 23 in order to obtain an average over N sample values. The obtained average of the actual arrival times is supplied to a correction control means 24 together with the receiving clock. The
20 correction control means 24 generates a control signal in accordance with the above equation (5). Thus, it essentially works as a time difference calculator.

The above described detecting means 20 according to Fig. 5
25 may be implemented by discrete hardware components or by a CPU which is controlled on the basis of a control program.

In case of a hardware implementation, the correction control means 24 may comprise a phase detector which may operate as
30 follows.

If the time difference is positive, i.e. the actual arrival time is shorter than the expected arrival time ($\Delta t_e < \Delta t_r$), a pulse of a first polarity (e.g. positive pulse) is generated as the control signal, and if the result is negative, i.e.

5 $\Delta t_e > \Delta t_r$, a pulse of a second polarity (e.g. negative polarity) is generated. These pulses are used to control the VCO 40. Thus, only a comparison between the time intervals Δt_e and Δt_r is actually required in order to correct the clock frequency of the receiver 2.

10

In summary, a clock generating method and apparatus for an asynchronous transmission are disclosed, wherein a plurality of actual receiving signal arrival times are detected and averaged, to thereby avoid influences of randomly distributed
15 delay variations upon signal transmission. Clock synchronization between a transmitting clock and a receiving clock is obtained by correcting the receiving clock on the basis of the obtained average of the actual arrival times and an expected arrival time. Thereby, overflow and underflow of
20 a receiver buffer can be prevented.

It should be understood that the above description and accompanying figures are only intended to illustrate the present invention. Thus, the method and apparatus according
25 to the invention may also be used in systems other than the described GSM system. The preferred embodiment of the invention may thus vary within the scope of the attached claims.

Claims:

1. A clock generating method for an asynchronous transmission, comprising the steps of:
determining a plurality of actual signal arrival times;
averaging said plurality of actual signal arrival times; and
correcting a timing of a receiving clock on the basis of said average of the signal arrival times and an expected signal arrival time.
2. A method according to claim 1,
wherein said expected signal arrival time is derived from said receiving clock.
3. A method according to claims 1 or 2,
wherein said determining step comprises counting a time period between the arrival of a first and the arrival of a subsequent second signal.
4. A method according to claim 3,

wherein said averaging step comprises storing said counted time periods and calculating an average of said stored time periods.

5 5. A method according to any one of the preceding claims,
wherein said correcting step comprises determining a
difference between a frequency corresponding to said average
of said plurality of actual signal arrival times and a
frequency of said receiving clock, and changing the frequency
10 of said receiving clock according to said frequency
difference.

6. A method according to any one of the preceding claims,
wherein the asynchronous transmission is an ATM
15 transmission and the signal is an ATM cell.

7. A clock generating apparatus for an asynchronous
transmission, comprising:
determining means (20) for determining an average of
20 actual signal arrival times and for generating a control
signal on the basis of said determined average of the actual
signal arrival times and an expected signal arrival time; and
correcting means (40) for correcting a timing of a
receiving clock on the basis of said control signal.

25

8. An apparatus according to claim 7,
wherein said correcting means comprises a voltage
controlled oscillator (40).

30 9. An apparatus according to claims 7 or 8,
wherein said determining means (20) comprises:

detecting means (21) for detecting an actual arrival time of a signal;

averaging means (23) for averaging a plurality of detected actual signal arrival times in order to obtain said
5 average of the actual signal arrival times; and

correction control means (24) for comparing said average of the actual signal arrival times with said expected signal arrival time and for generating said control signal in accordance with the comparison result, wherein said expected
10 signal arrival time is derived from said receiving clock.

10. An apparatus according to claim 9,
wherein said determining means (20) comprises storing means (22) for storing said plurality of detected actual
15 signal arrival times.

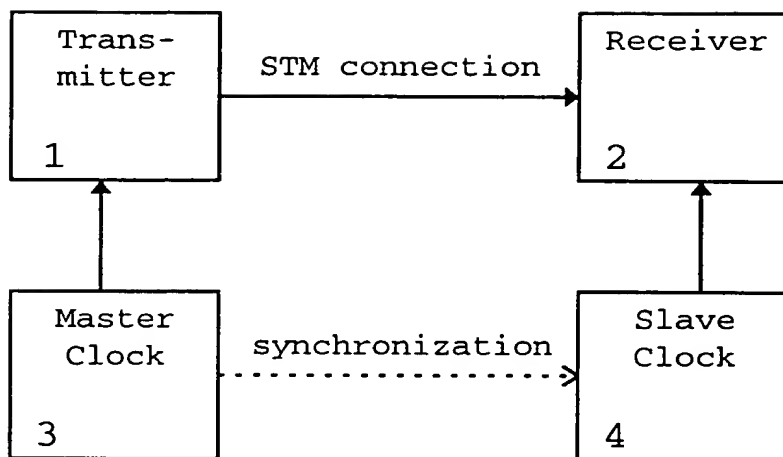
11. An apparatus according to claims 9 or 10,
wherein said detecting means (20) comprises timer.

20 12. An apparatus according to any one of claims 9 to 11,
wherein said correction control means (24) comprises a phase detector, and wherein a polarity of said control signal is changed in accordance with the result of comparison.

25 13. An apparatus according to any one of claims 7 to 12,
wherein the asynchronous transmission is an ATM transmission and the signal is an ATM cell.

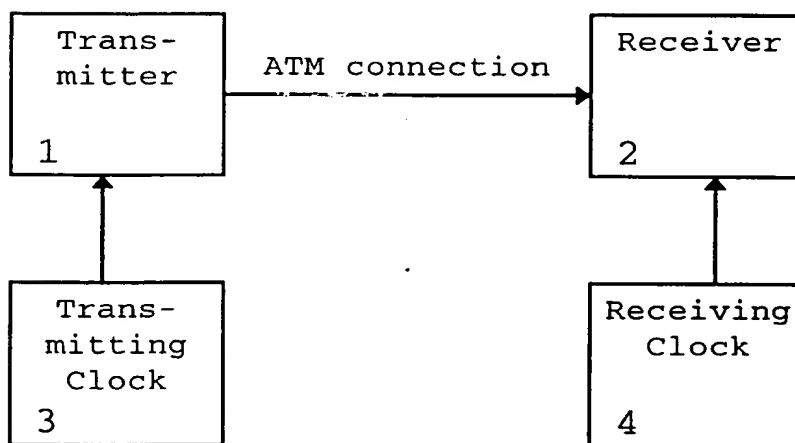
Abstract:

Clock generating method and apparatus for an asynchronous transmission, wherein a plurality of actual receiving signal arrival times are detected and averaged, to thereby avoid influences of randomly distributed delay variations upon signal transmission. Clock synchronization between a transmitting clock and a receiving clock is recovered by correcting the receiving clock on the basis of the obtained average of the actual arrival times and an expected arrival time. Thereby, overflow and underflow of a receiver buffer can be prevented.



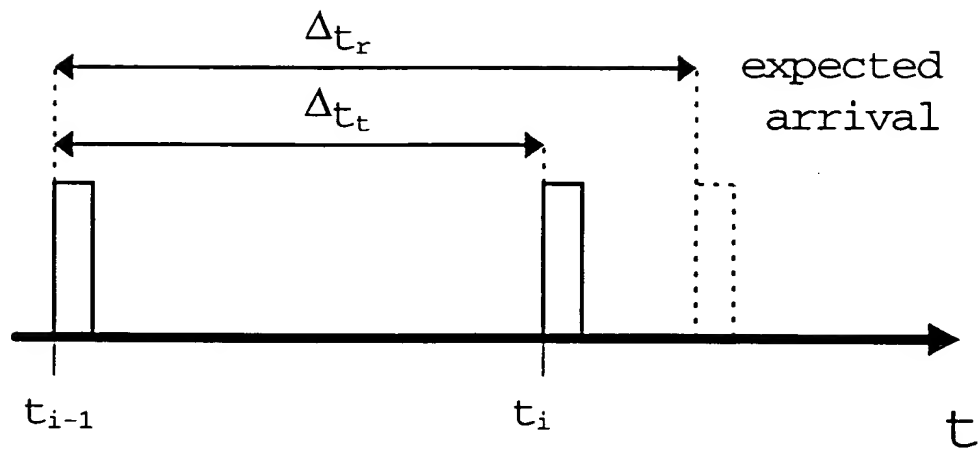
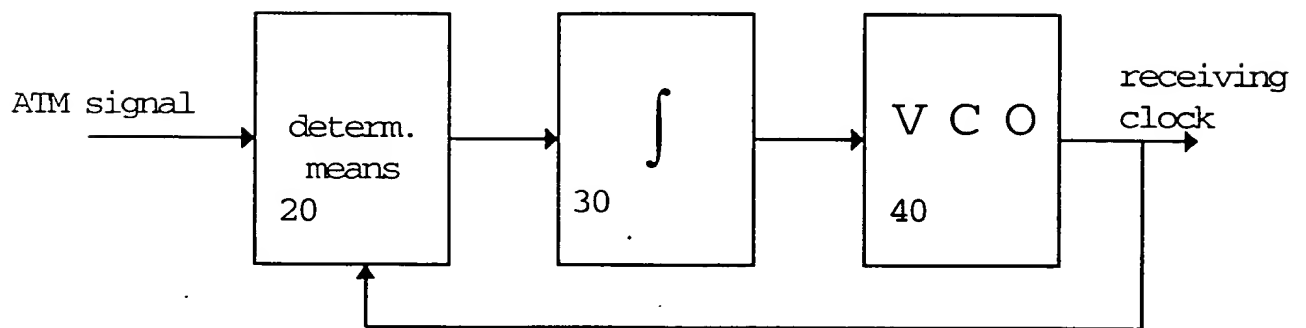
PRIOR ART

Fig. 1A



PRIOR ART

Fig. 1B

**Fig. 2****Fig. 3**

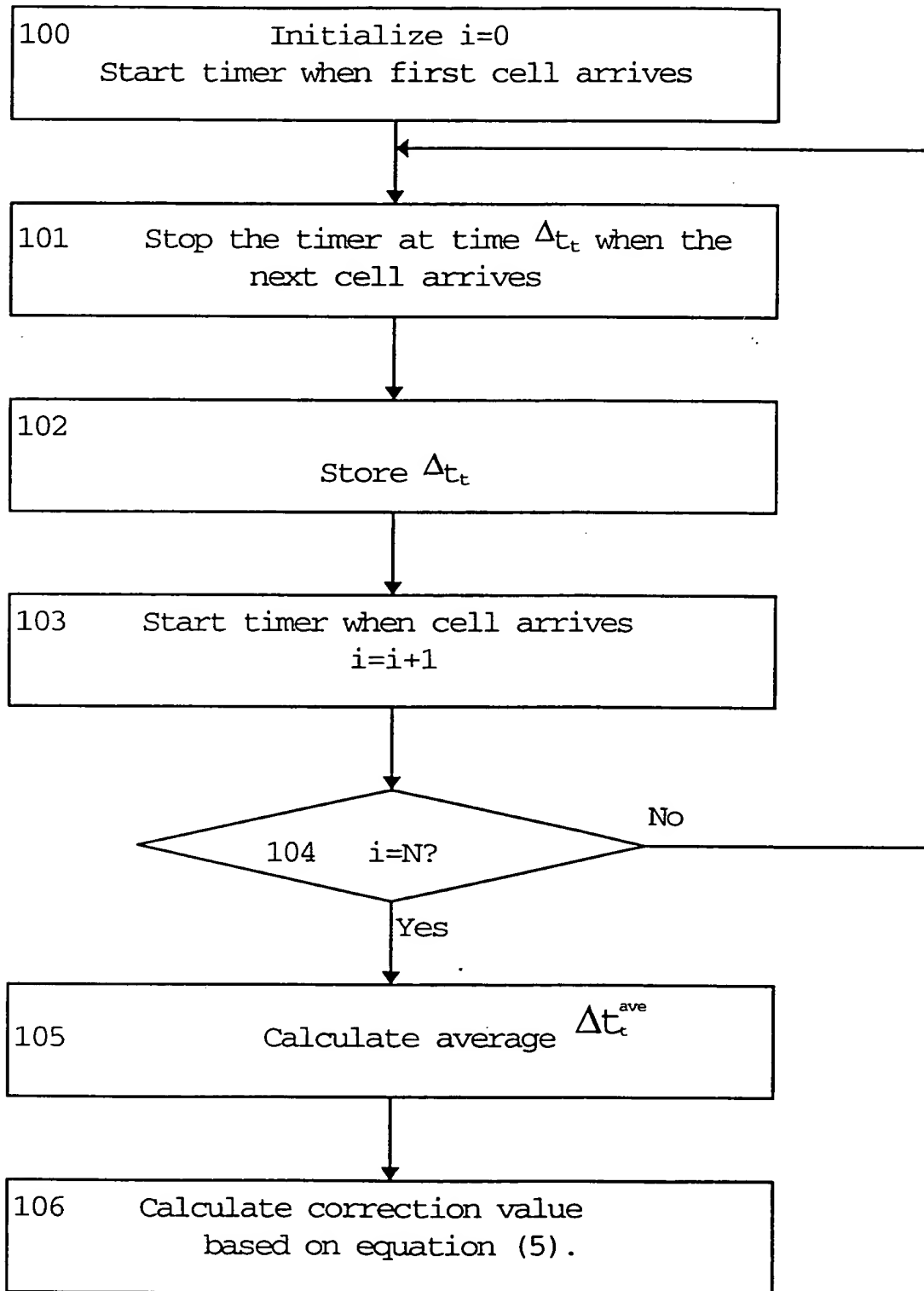


Fig. 4

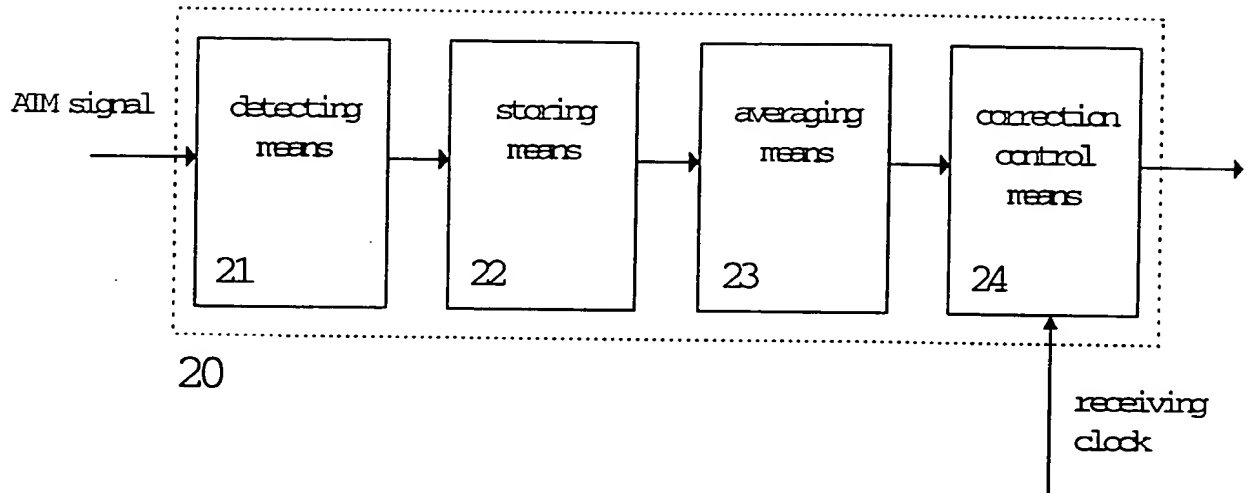


Fig. 5